Marshall University Syllabus

Course Title/Number  Computer Architecture/CS402
Semester/Year  Spring/2014
Days/Time  S201 CRN: 4740 MWF/10:00 - 10:50 AM
Location  GH206A
Instructor  Jonathan Thompson
Office  GH205C
Phone  (304)696-6349
E-Mail  thompsonj@marshall.edu
Office/Hours  GH205C/MWF 9:00 – 9:50a and 1:00 - 1:50p

University Policies  By enrolling in this course, you agree to the University Policies listed below. Please read the full text of each policy by going to www.marshall.edu/academic-affairs and clicking on “Marshall University Policies.” Or, you can access the policies directly by going to http://www.marshall.edu/academic-affairs/?page_id=802.

Academic Dishonesty / Excused Absence Policy for Undergraduates / Computing Services Acceptable Use / Inclement Weather / Dead Week / Students with Disabilities / Academic Forgiveness / Academic Probation and Suspension / Academic Rights and Responsibilities of Students / Affirmative Action / Sexual Harassment

Course Description: From Catalog
Design and analyze structure of major hardware components of computers including: ALU, instruction sets, memory hierarchy, parallelism through multicore and many core, storage systems and interfaces. PR: CS300.
## Course Student Learning Outcomes

The table below shows the following relationships: How each student learning outcomes will be practiced and assessed in the course.

<table>
<thead>
<tr>
<th>Course Student Learning Outcomes</th>
<th>How students will practice each outcome in this Course</th>
<th>How student achievement of each outcome will be assessed in this Course</th>
</tr>
</thead>
<tbody>
<tr>
<td>A knowledge of, and an ability to describe the mechanics of how hardware and system software execute the programs that you write</td>
<td>In class lab exercises</td>
<td>Completion of lab exercises</td>
</tr>
<tr>
<td></td>
<td>Ungraded homework assignments</td>
<td>Graded quiz questions</td>
</tr>
<tr>
<td></td>
<td>In class examples</td>
<td>Graded exam problems</td>
</tr>
<tr>
<td>A knowledge of, and an ability to describe the interaction among the various components of the cpu and of a computer system</td>
<td>In class lab exercises</td>
<td>Completion of lab exercises</td>
</tr>
<tr>
<td></td>
<td>Ungraded homework assignments</td>
<td>Graded quiz questions</td>
</tr>
<tr>
<td></td>
<td>In class examples</td>
<td>Graded exam problems</td>
</tr>
<tr>
<td>An ability to control external I/O devices from the CPU and to create an integrated microcontroller-based system</td>
<td>In class lab exercises</td>
<td>Completion of lab exercises</td>
</tr>
</tbody>
</table>

## Required Texts, Additional Reading, and Other Materials

### Required Text


### Other Materials

- **Arduino Prototyping Platform**
  - [www.arduino.cc](http://www.arduino.cc)
- **MARS MIPS Simulator**
  - [courses.missouristate.edu/kenvollmar/mars/](http://courses.missouristate.edu/kenvollmar/mars/)
- **ChipKIT Uno32 Documentation**
  - [www.digilentinc.com](http://www.digilentinc.com)

### Other Texts

Course Requirements / Due Dates

In-Class Quizzes
The quizzes cover material from the assigned textbook. They are on-line and must be taken during the class period. Each quiz consists of six questions randomly selected from a pool of twenty practice quiz questions. Practice quizzes will be made available a week before the quiz and you may take them as many times as you wish.

Lab Exercises
These give you the opportunity to apply the material covered in the textbook and the lectures. They will be graded as P (done) or F (not done).

Homework
Assignments will be graded using the following point system: 3 points - good, 2 points - fair, 1 point - poor, and 0 points - not submitted. Late submissions will not be accepted.

Interim Examinations
There will be two interim exams during the semester. Only University Excused Absences will be accepted for make-up examinations.

Final Exam
There will be a comprehensive two-hour final exam.

Due Dates
See the Course Schedule on page four for due dates.

Grading Policy

<table>
<thead>
<tr>
<th>Activity</th>
<th>Points</th>
</tr>
</thead>
<tbody>
<tr>
<td>Class Attendance, Participation, and Decorum</td>
<td>10</td>
</tr>
<tr>
<td>Quizzes</td>
<td>20</td>
</tr>
<tr>
<td>Lab Exercises</td>
<td>15</td>
</tr>
<tr>
<td>Homework</td>
<td>5</td>
</tr>
<tr>
<td>Exam 1</td>
<td>15</td>
</tr>
<tr>
<td>Exam 2</td>
<td>15</td>
</tr>
<tr>
<td>Final Exam</td>
<td>20</td>
</tr>
<tr>
<td>Total</td>
<td>100</td>
</tr>
</tbody>
</table>

Course grade is awarded based on the following scheme:

<table>
<thead>
<tr>
<th>Score</th>
<th>Letter Grade</th>
</tr>
</thead>
<tbody>
<tr>
<td>&gt;= 90</td>
<td>A</td>
</tr>
<tr>
<td>&gt;= 80 &amp; &lt; 90</td>
<td>B</td>
</tr>
<tr>
<td>&gt;= 70 &amp; &lt; 80</td>
<td>C</td>
</tr>
<tr>
<td>&gt;= 60 &amp; &lt; 70</td>
<td>D</td>
</tr>
<tr>
<td>&lt; 60</td>
<td>F</td>
</tr>
</tbody>
</table>

Attendance Policy
Attendance will be taken at the start of class. Only University Excused Absences will be accepted.
## Course Schedule

Any revisions to this schedule will be posted on MUOnline.

<table>
<thead>
<tr>
<th>Wk</th>
<th>Monday</th>
<th>Wednesday</th>
<th>Friday</th>
</tr>
</thead>
</table>
| 1  | 13-Jan: Course Introduction  
Read: Ch 1.1 - 1.3 | 15-Jan: Computer Architecture  
Read: Ch 2.1 - 2.5 | 17-Jan: Performance Assessment  
Read: Ch 2.6 |
| 2  | 20-Jan: No Class  
Martin Luther King Birthday | 22-Jan: Computer Function  
Read: Ch 3.1 - 3.2  
Quiz: Ch 1 | 24-Jan: System Interconnections  
Read: Ch 3.3 - 3.5  
HW1 Due |
| 3  | 29-Jan: PCIe Bus  
Read: Ch 3.6  
Lab1: ChipKIT Setup  
Quiz: Ch 2 | 29-Jan: Lab2: Controlling LEDs  
Read: Ch 3.6  
Lab1: ChipKIT Setup | 31-Jan: Computer Memory  
Read: Ch 4.1 - 4.2  
HW2 Due  
Quiz: Ch 3 |
| 4  | 03-Feb: Cache Memory Design  
Read: Ch 4.3  
Quiz: Ch 4 | 05-Feb: Lab3: LCD Controller  
Quiz: Ch 4 | 07-Feb: Internal Memory  
Read: Ch 5.1 - 5.3  
HW3 Due |
| 5  | 14-Feb: HW3 Review  
Quiz: Ch 5 | 12-Feb: Exam 1  
Ch 1 - 5 | 14-Feb: External Memory  
Read: Ch 6.1 - 6.5 |
| 6  | 17-Feb: External Devices  
Read: Ch 7.1 - 7.5  
Quiz: Ch 6 | 19-Feb: DMA, I/O Channels  
Read: Ch 7.5 - 7.6  
Exam 1 Results | 21-Feb: Number Systems  
Read: Ch 9.1 - 9.5, 10.1 - 10.2  
HW4 Due |
| 7  | 24-Feb: Integer Arithmetic  
Read: Ch 10.3  
Quiz: Ch 7 | 26-Feb: FP Representation  
Read: Ch 10.5 | 28-Feb: Lab4: HW Interrupts  
HW5 Due |
| 8  | 03-Mar: FP Arithmetic  
Read: Ch 10.6 | 05-Mar:  
Quiz: Ch 9 | 07-Mar: Boolean Algebra, Gates  
Read: Ch 11.1 - 11.2  
HW6 Due |
| 9  | 10-Mar: Combinatorial Circuits  
Read: Ch 11.3  
Quiz: Ch 10 | 12-Mar: Lab5: Bits and Bytes | 14-Mar: Sequential Circuits  
Read: Ch 11.4 - 11.5  
HW7 Due |
| 10 | 24-Mar:  
Quiz: Ch 11 | 26-Mar: Exam 2  
Ch 6 - 7, 9-11 | 28-Mar: Machine Instructions, Operands, Op Types  
Read: Ch 12.1, 12.2, 12.4, 12App  
HW8 Due |
| 11 | 31-Mar: Addressing Modes  
Read: Ch 13.1, 13.3, 13.5 | 02-Apr: MIPS ISA  
Exam 2 Results | 05-Apr: MIPS ISA  
HW9 Due |
| 12 | 07-Apr: Processor Organization  
Read: Ch 14.1 - 14.3  
Quiz: Ch 12 | 09-Apr: Lab6: MIPS Simulator  
Quiz: Ch 13 | 11-Apr: Pipelining  
Read: Ch 14.4  
HW10 Due |
| 13 | 14-Apr: Instruction Parallelism  
Read: Ch 16.1 - 16.2 | 16-Apr: Lab7: ChipKIT Assembler  
Quiz: Ch 14 | 19-Apr: Multiprocessors  
Read: Ch 17.1 - 17.2  
HW11 Due |
| 14 | 21-Apr: Cache Coherence  
Read: Ch 17.3 - 17.4 | 23-Apr: Lab8: R/W Memory, EEPROM  
Quiz: Ch 16 | 25-Apr: Clusters  
Read: Ch 17.5 - 17.6  
HW12 Due |
| 15 | 28-Apr: Vector Computation  
Read: Ch 17.7 | 30-Apr: Multicore  
Read: Ch 18  
Quiz: Ch 17 | 02-May: Last Class  
Quiz: Ch 18 |
| 16 | 05-May: Final Exam  
10:15 - 12:15 GH206A | | |